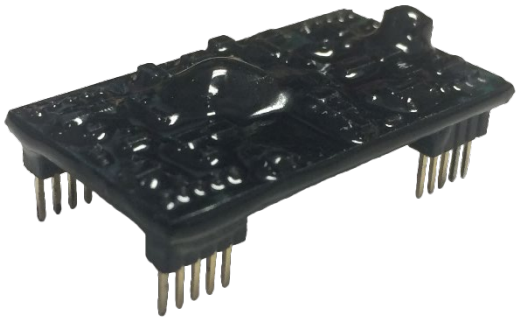

Size: 1.25in x 0.70in x 0.31in (31.8mm x 17.8mm x 7.9mm)

FEATURES

- Epoxy Coating
- Compact Package
- Several Outputs Voltages Available (Contact Factory for more information)
- Through Hole Package
- Dual Output
- 1000VDC Isolation
- Low Power

DESCRIPTION

The XNED3954 provides an isolated primary and secondary HIGH pulse (or open collector LOW) that can be used to turn on a MOSFET or Thyristor to shut down and discharge a power supply in the event of a nuclear blast. The XNED3954 is designed to survive the nuclear environment while sensitive electronics cannot, and must be de-energized. The pulse duration of the XNED3954 can be increased with the addition of ceramic capacitors at the V_{xhld} pin. The output pins will continue to provide the output HIGH (or LOW) as long as the hold-up time even with the removal of primary and secondary input. Customization available.

XNED3954 PIN Assignments

Pin	Name	Function	Description
Pin 1	VPRI_input	Primary side input	
Pin 2	VPHLD	Input Hold-up Capacitor	Adding additional capacitance to this pin increases the primary side time HIGH duration at NEDp. If additional hold up is not desired, leave pin unconnected. See Equation 2 for value. Vphld is referenced to the GND.
Pin 3	NEDP	Primary side referenced output	Provides output high after NED event. Once triggered, NEDp stays high as long as input Vpri is maintained. NEDp is referenced to the GND.
Pin 7	VSEC_input	Secondary side input	
Pin 8	VSHLD	Output Hold-Up Capacitor	Adding additional capacitance to this pin increases the secondary side time HIGH duration at NEDs. If additional hold up is not desired, leave pin unconnected. See Equation 1 for value. Vshld is referenced to Vsec_rtn. Note: primary holdup time must be greater than secondary holdup time.
Pin 9	VSFLAG	Input power for FLAG output	Input for FLAG output. VsFlag is referenced to Vsec_rtn
Pin 10	NEDS	Secondary side referenced output	Provides output high after NED event. NEDs stays high as long as inputs Vpri and Vsec are maintained. NEDs is referenced to Vsec_rtn.
Pin 11	FLAG-RST	FLAG Reset	LOW resets FLAG output after NED event. Note that first NED_rst must be cycled or input power removed before FLAG_rst will reset FLAG. Flag_rst is referenced to Vsec_rtn.
Pin 12	FLAG	FLAG Output	Provides high output after NED event. Stays high as long as VsFlag is high. Does not get reset if Vpri or Vsec removed. FLAG is resourced from VsFlag and referenced to Vsec_rtn.
Pin 13	NEDSOC	Secondary side referenced open-connector output	Provides open-collector output LOW after NED event. NEDsoc is referenced to Vsec_rtn.
Pin 14	Vsec_RTN	Secondary side return	
Pin 17	NEDPOC	Primary side referenced open-collector output	Provides open-collector output LOW after NED event. NEDpoc is referenced to the GND.
Pin 18	NED-RST	NED Reset	HIGH resets NET detector (NEDp & NEDs) after NED event.
Pin 19	NED-TST	NED Test	HIGH causes a NED even to trigger. NED_tst is referenced to the GND.
Pin 20	Vprim_RTN	Primary side return	

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website: www.wallindustries.com • e-mail: sales@wallindustries.com

SPECIFICATIONS: XNED3954

All specifications are based on 25°C, Nominal Input Voltage, and Maximum Output Current unless otherwise noted.
We reserve the right to change specifications based on technological advances.

SPECIFICATION	PIN	TEST CONDITIONS	Min	Typ	Max	Unit
PRIMARY						
Operating Voltage Range	Vpri		16	28	36	Vdc
Input Supply Current	Vpri	NEDp LOW	-	0.4	1.3	mA
Input Supply Current	Vpri	NEDp HIGH; I_{NEDp}=3mA	-	6	9	mA
Input Surge Voltage	Vpri	1s max.	-	-	75	VDC
Output Resistance	NEDp	V_{pri}=0V	-	100	-	KΩ
Output Voltage Range	NEDp		4.5	5.0	6.0	Vdc
DC Output Current	NEDp		-	-	5	mA
Peak Output Current	NEDp	500uS Max.; C_{phld}=0uF	-	-	20	mA
Delay NED_tst to NEDp	NEDp	Photo 1; V_{pri}=28Vdc, I_{NEDp}=3mA	-	0	-	µs
NEDp Rise Time	NEDp	Photo 1; V_{pri}=28Vdc, I_{NEDp}=3mA	-	2	-	µs
NEDp Hold-Up Time	NEDp	Photo 2; V_{pri}=16Vdc, I_{NEDp}=3mA, C_{phld}=0uF	-	2.4	-	ms
Max. Voltage	NEDpoc		-	-	36	Vdc
Max. Sink Current	NEDpoc		-	-	73	mA
Max. Input Voltage	NED_tst		-	-	20	Vdc
	NED_rst		-	-	10	Vdc
Min. On Time	NED_tst		10	-	-	µs
	NED_rst					
SECONDARY						
Operating Voltage Ranges	Vsec		4	-	8	Vdc
Input Supply Current	Vsec	NEDs LOW	-	20	50	µA
Input Supply Current	Vsec	NEDs HIGH; I_{NEDs}=3mA	-	2.5	7.5	mA
Input Surge Voltage	Vsec	1s max.	-	-	16	Vdc
Output Resistance	NEDs	V_{sec}=0V	-	100	-	KΩ
Output Voltage Range	NEDs		-	V_{sec}-1	-	Vdc
Max. Output Current	NEDs		-	-	20	mA
Delay NED_tst to NEDs	NEDs	Photo 2; V_{sec}=5Vdc, I_{NEDs}=20mA	-	1	-	µs
NEDs Rise Time	NEDs	Photo 2; V_{sec}=5Vdc, I_{NEDs}=20mA	-	8	-	µs
NEDs Hold-Up Time	NEDs	Photo 4; V_{sec}=5Vdc, I_{NEDs}=20mA,C_{shld}=0uF	-	100	-	µs
Max. Voltage	NEDsoc		-	-	36	Vdc
Max. Sink Current	NEDsoc		-	-	73	mA
FLAG						
Operating Voltage Range	VsFlag		4	-	8	Vdc
Input Supply Current	VsFlag	FLAG LOW	-	0	-	µA
Input Supply Current	VsFlag	FLAG HIGH; V_{sFlaq}=5Vdc, I_{FLAG}=0mA	-	25	-	µA
Output Voltage Range	FLAG		-	-	V_{sFlag}	Vdc
Max. Output Current	FLAG	Photo 3; V_{sFlag}=5Vdc, I_{FLAG}=1mA	-	-	50	mA
Delay NED_tst to FLAG	FLAG	Photo 3; V_{sFlag}=5Vdc, I_{FLAG}=1mA	-	6	-	µs
FLAG Rise Time	FLAG	Photo 3; V_{sFlag}=5Vdc. I_{FLAG}=1mA	-	0	-	µs
FLAG Hold-Up Time	FLAG	with External Source	-	-	∞	s
Max. Input Voltage	FLAG_rst		-	-	10	Vdc
Min. On Time	FLAG_rst		10	-	-	µs
ISOLATION						
Primary-Secondary	1 minute		1000			Vdc
THERMAL						
Operating Ambient			-55	-	125	ºC
Storage Temperature			-55	-	150	ºC

NOTES

1. Other output voltages are available. Please contact factory for more information.

**Due to advances in technology, specifications subject to change without notice.*

EQUATIONS

Equation 1: Calculation of C_{shld}

$$t_{NEDs} = (C_{shld} + 10uF) \times \frac{\Delta V_{NEDs}}{(I_{Neds} + 3mA)}$$

Example: for a ΔV_{NEDs} of 0.1V and a load of 10mA

$t_{NEDp} > t_{NEDs}$

Cshld=10V

C_{shld}	t_{NEDs}
0 µF	77 µs
10 µF	154 µs
20 µF	231 µs
30 µF	308 µs
40 µF	385 µs
50 µF	462 µs
100 µF	846 µs

Equation 2: Calculation of C_{phld}

$$t_{NEDp} = C_{phld} \times \frac{{V_{PRI}}^2 - 169}{11.2 \times (I_{Nedp} + 4mA)}$$

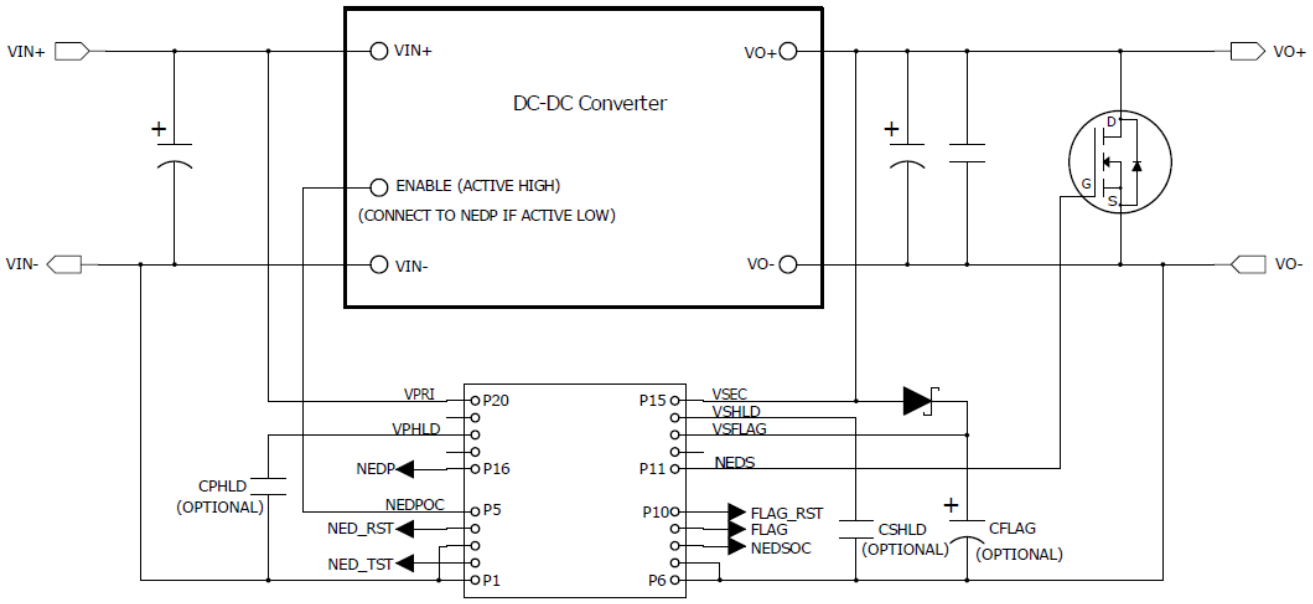
Example: for a minimum V_{pri} input of 16V and a load of 3mA

C_{phld} = 50V

C_{phld}	t_{NEDp}
0 µF	2.4 ms
1 µF	3.5 ms
2 µF	4.6 ms
3 µF	5.7 ms
4 µF	6.8 ms
5 µF	7.9 ms
10 µF	13.5 ms

TYPICAL APPLICATION CIRCUIT

Typical XNED3954 Application Circuit



PHOTOS

Photo 1: NEDp (Yellow) Turn On Delay and Rise Time vs NED_tst (Blue)

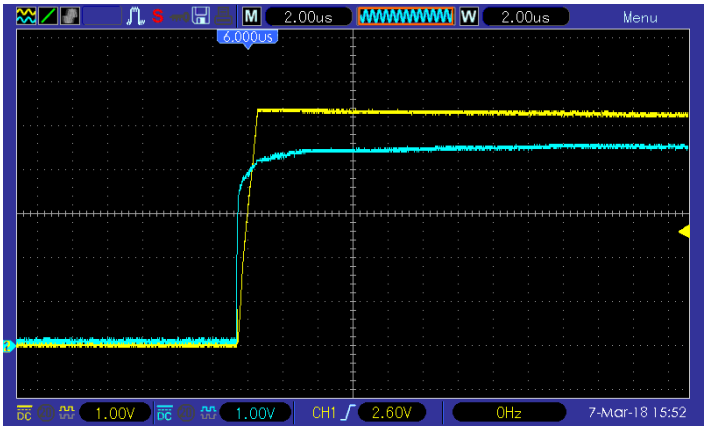


Photo 2: NEDp (Yellow) Hold Up Time while disabling Vpri (BLUE); C_{phld}=0uF

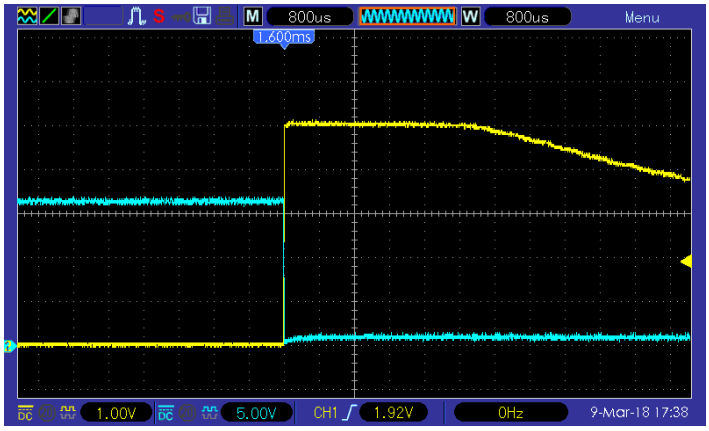


Photo 3: NEDs (Yellow) Turn On Delay and Rise Time vs NED_tst (Blue)

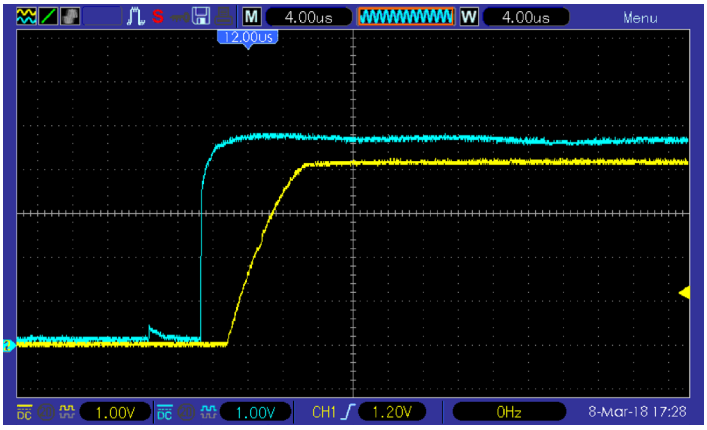


Photo 4: NEDs (Yellow) Hold Up Time while disabling Vsec (BLUE); C_{shld}=0UF

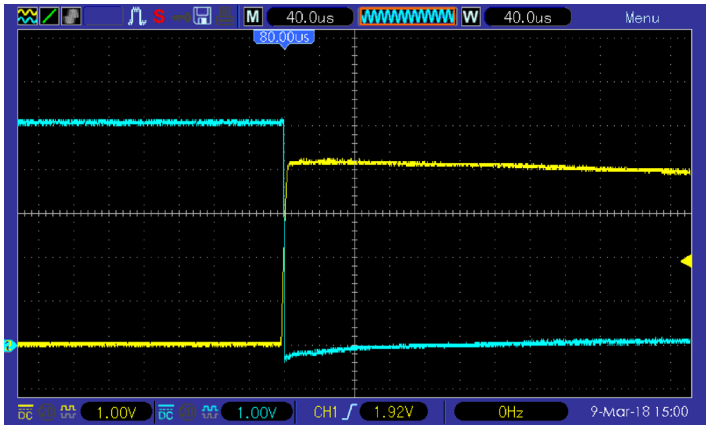
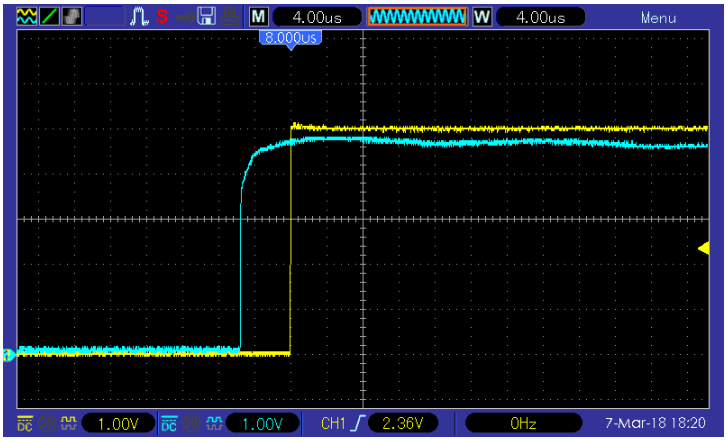
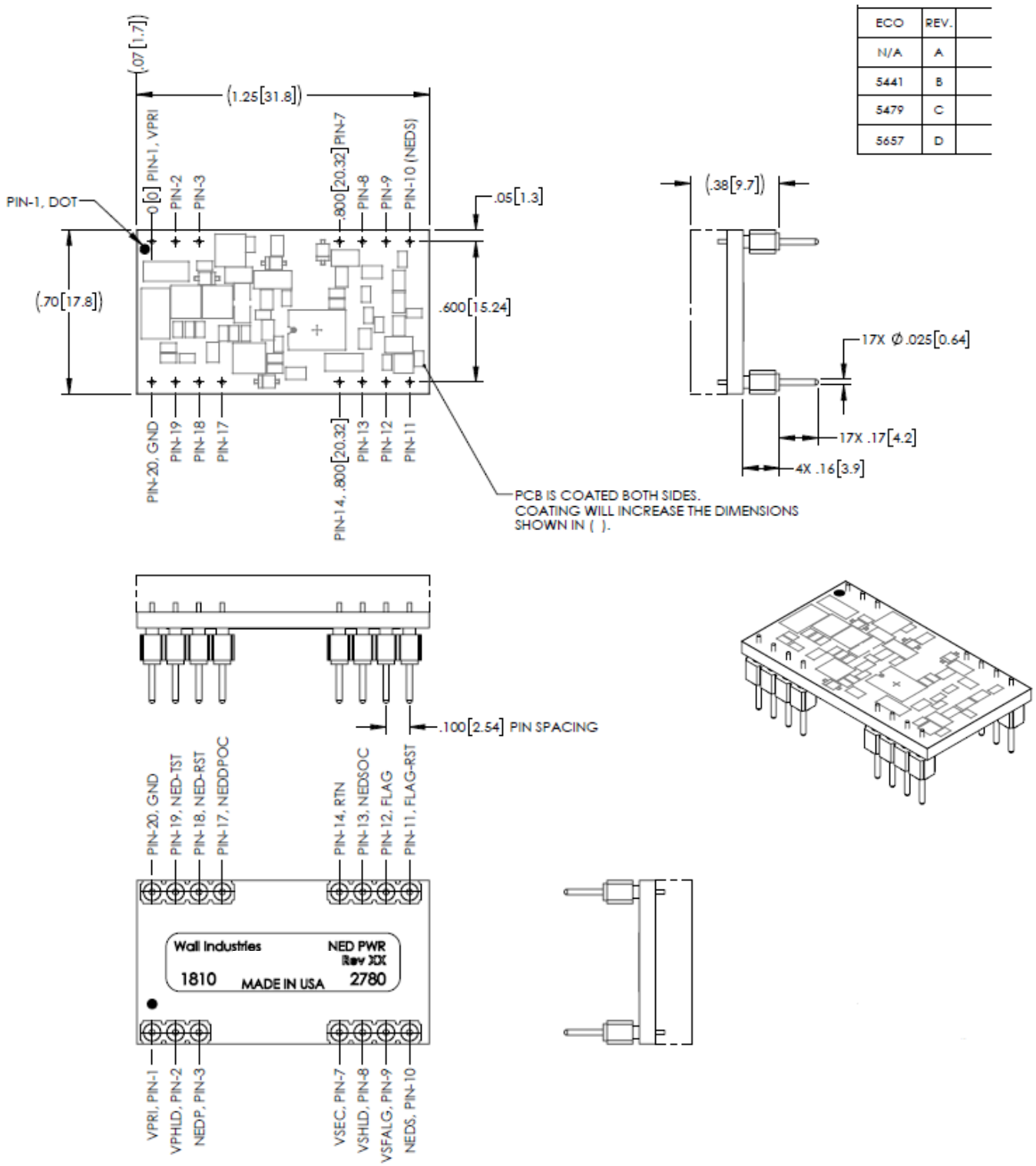


Photo 5: FLAG (Yellow) Turn On Delay and Rise Time vs. NED_tst (Blue)



MECHANICAL DRAWINGS



COMPANY INFORMATION

Wall Industries, Inc. has created custom and modified units for over 50 years. Our in-house research and development engineers will provide a solution that exceeds your performance requirements on-time and on budget. Our ISO9001: 2015 certification is just one example of our commitment to producing a high quality, well-documented product for our customers.

Our past projects demonstrate our commitment to you, our customer. Wall Industries, Inc. has a reputation for working closely with its customers to ensure each solution meets or exceeds form, fit and function requirements. We will continue to provide ongoing support for your project above and beyond the design and production phases. Give us a call today to discuss your future projects.

Contact **Wall Industries** for further information:

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